REMARKS

Claims 1-7 and 9-36 are pending in the application.

Claims 1-7 and 9-36 stand rejected.

Claims 9-11, 27, 30, and 33-36 have been amended. No new matter has been added by these amendments.

Claim Objections

In the Office Action mailed June 30, 2006 (hereinafter referred to as "Office Action"), claims 9-12 are objected to under 37 C.F.R. §1.75(c), as being in improper dependent form because they are, directly or indirectly, dependent on cancelled claim 8. Office Action, p. 2. Claims 9-11 have been amended to depend from claim 1. Claim 12 depends from amended claim 11. Accordingly, Applicant asserts that this objection has been overcome.

Rejection of Claims under 35 U.S.C. §112

Claims 33-35 stand rejected under 35 U.S.C. §112, first paragraph, for failing to comply with the enablement requirement. Office Action, p. 3. Applicant has amended claim 33 so that, as amended, the computer program product of claim 33 includes a tangible computer readable medium that encodes the first set of instructions. By rewriting the claim in this manner, Applicant has removed the language at issue in the §112 rejection. Accordingly, Applicant believes that this rejection is now moot.

Rejection of Claims under 35 U.S.C. §101

Claims 30-35 stand rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. In particular, the Examiner pointed out that claims 30-35 might not be limited to tangible embodiments. Office Action, pp. 3-4. With respect to claims 30-32, Applicant notes that these claims require a processor, which is inherently tangible. Accordingly, Applicants assert that this rejection does not appear to apply to claims 30-32.

In order to address the concern about tangibility in claims 33-35, Applicant has explicitly added the word "tangible" to claim 33. Applicant therefore asserts that this rejection has been overcome.

Rejection of Claims under 35 U.S.C. §102

Claims 1, 3-7 and 9-36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kashima et al. (USPN: 5,485,598) hereinafter referred to as "Kashima." Applicant respectfully traverses this rejection.

Claim 36 recites: "maintaining a first cache and a second cache, wherein said maintaining is performed by one of an upper-level system and a lower-level system" and "providing access to said second cache by the other of said upper-level system and said lower-level system." As noted in the prior response (submitted with the RCE mailed June 15, 2006), Kashima does not teach these features of claim 36.

In the Advisory Action mailed May 12, 2006 (hereinafter referred to as "Advisory Action"), the Examiner equates the upper-level system of claim 36 with the main memory system of Kashima, while also equating the lower-level system of claim 36 with the disk array of Kashima. Advisory Action, p. 2. The cited art teaches a system in which the old data cache can be part of the main memory system (e.g., as shown in FIGs. 8 and 11 of Kashima) or part of a disk array (e.g., as shown in FIGs. 4 and 14 of Kashima). However, the description of these configurations does not teach or suggest a scenario in which either the main memory system maintains the old data cache, while access to the old data cache is provided to the disk array, or the disk array maintains the old data cache, while access to the old data cache is provided to the main memory system.

In the description of FIG. 6, which is a flowchart describing how the system of FIG. 4 (in which the disk array includes the old data cache) operates, Kashima describes how the disk array writes information into the old data cache and reads information from the old data cache. In this example, the main memory system does not have access to the old data cache. Kashima, col. 4, lines 13-18 and 33-39.

Similarly, in the description of FIG. 10, which is a flowchart describing how the system of FIG. 8 (in which the main memory system includes the old data cache) operates, Kashima

describes how the OS copies information into the old data cache and transfers information from the old data cache to the disk array for use in the generation of the new checksum (CK) data. Kashima, col. 5, lines 21-25 and 32-37. In this example, the disk array must rely on the OS to transfer the data from the old data cache to the disk array.

Applicants note that simply receiving data that might have, at one point, been stored in a cache does not teach that the recipient has "access" to the cache. Access implies that the device having access is able to initiate an operation that reads from and/or writes to the cache (as opposed to simply receiving data has been read from and/or written to the cache). Thus, in the example described with respect to FIG. 10 of Kashima, only the OS has access to the old data cache. The disk array, while able to receive data that was stored in the old data cache, does not have access to old data cache itself. Accordingly, for at least the foregoing reasons, the cited portions of Kashima fail to teach or suggest "maintaining a first cache and a second cache, wherein said maintaining is performed by one of an upper-level system and a lower-level system" and "providing access to said second cache by the other of said upper-level system and said lower-level system," as recited in claim 36.

On page 14 of the current Office Action, the Examiner states:

> Kashima does teach about maintaining the first and second caches by the upper-level system (i.e., the main memory 12 in Fig. 4). Furthermore, in the system taught by Kashima, the lower level system (i.e., the disk array 2a-2d in Fig. 4) has to have an access to the second cache for at least one/some time so it (the disk array) can copy/transfer the data from the second cache before the second cache get updated.

However, no portion of Kashima has been cited in support of the above position. Furthermore, Applicant notes that in Fig. 4 of Kashima, the old data cache (equated with the second cache of claim 36) is part of (and maintained and accessed by, as described in Fig. 6 of Kashima) the disk array. Thus, in the version of Kashima's system shown in Fig. 4, only the disk array has access to the old data cache. This is supported by Fig. 6, which clearly describes any activity that accesses the old data cache as being performed by the disk array, not the OS (e.g., steps S8, S9, and S12 are performed by the disk array). Clearly, Fig. 4 fails to support the Examiner's position. Also, Applicant notes that the mere fact that Kashima's figures show the old data cache (included within the disk array) being indirectly connected to the main memory has nothing to do with whether the main memory has the ability access to the old data cache.

Furthermore, the Examiner's assertion that the lower level system has to have access to the old data cache (when the old data cache is maintained by the upper level system) so that the lower level system can copy data from the old data cache before the old data cache is updated is simply not true. Instead, before modifying the old data cache, the upper level system can read data from the old data cache and transfer this information to the lower level system. Applicant notes that this is consistent with the descriptions in Kashima where, when the old data cache is maintained in the same system as the disk cache (e.g., as shown in Fig. 8), the OS (not the disk array) transfers data from the old data cache to disk array. *See, e.g.,* step S11 in Fig. 10 of Kashima.

Rejection of Claims under 35 U.S.C. §103

Claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kashima. Applicant respectfully traverses this rejection, for at least the foregoing reasons presented above with respect to claim 36.

Further with respect to claim 2, Applicant notes that, regardless of whether it is well-known in the art to integrate certain types of caches, it is not well known to integrate caches such as those described in claim 2. In particular, claim 2 describes a single cache that includes both a first cache and a second cache, the latter of which is maintained by either an upper-level system or a lower-level system and also able to be accessed by the other of the upper-level system or the lower-level system, as described in claim 36 (from which claim 2 depends). While the rejection addresses the general concept of combining two caches, no teachings or suggestions have been provided as to why one would integrate the two caches described in claim 36, which have specifically claimed functionality (e.g., the ability of the second cache to be maintained by one system while also capable of being accessed by another system).

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 29, 2006.

Attorney for Applicant(s) 9-29-2006 Date of Signature

Respectfully submitted,

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